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S/N 10/679,593 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Deshanand Singh et al.	Examiner: Tat, Binh C
Serial No.:	10/679,593	Group Art Unit: 2825
Filed:	October 6, 2003	Docket No.: ALT.P024 (A01002)
Title:	Method and Apparatus for Performing Layout-Driven Optimizations on Field Programmable Gate Arrays	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE – EXAMINING GROUP 2825

Dear Sir or Madam,

In response to the Office Action mailed January 7, 2009, Applicants respectfully request the Examiner to consider the following remarks.

PAGE 2/22 * RCVD AT 4/7/2009 3:43:19 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/38 * DNIS:2738300 * CSID:2173567373 * DURATION (mm-ss):03-26